WHITE PAPER

Probing Techniques for High-speed Protocol Analyzers

Passive versus Active Front-End Implementations

Introduction

With the wide adoption of high-speed serial bus technologies such as USB, PCI Express, SAS, and SATA, signal probing techniques are becoming more complex. Historically non-intrusive signal probing techniques were commonly used in most protocol analysis tools. However, rapid increases in bus speeds present numerous technical challenges. That requires the use of active repeaters to probing high-speed signals. This article provides an overview of protocol analyzers and explores the probing design techniques used in today's high-speed protocol analysis solutions, such as the Beagle™ USB 5000 SuperSpeed Protocol Analyzer.

What is a protocol analyzer?

A protocol analyzer is an analysis tool that is most often implemented as a combination of capture and processing hardware and analysis software. Protocol analyzers monitor the bus traffic on a bus, interpret the data by leveraging a deeper understanding of the underlying protocol, and display the results in a simplified yet comprehensive manner.

While oscilloscopes focus on the electrical and timing characteristics of a signal, protocol analyzers focus on the analysis of the link, protocol, driver, and applications layers. Protocol analyzers are becoming increasingly popular as they provide a significant cost advantage over competing solutions such as logic analyzers.

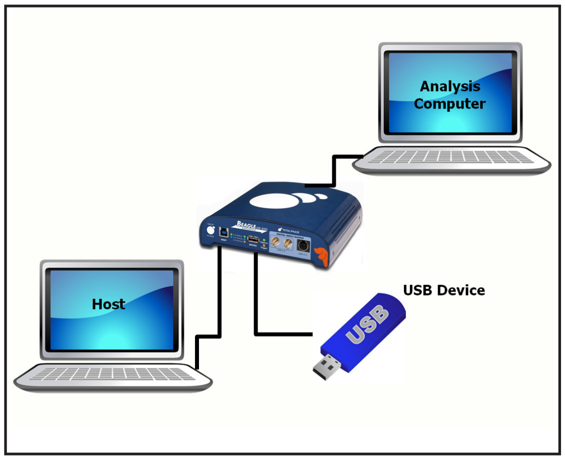

Figure 1: Typical Analyzer Setup

In a typical scenario such as Universal Serial Bus (USB), the protocol analyzer sits in between the host and device, monitors the traffic, and uploads the captured data to a personal computer for analysis and display. Figure 1 shows a typical configuration of a protocol analyzer set up.

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Protocol Analyzer Building Blocks

The core components of a protocol analyzer include (Figure 2):

1. **Front-end**: Serves as the primary interface of the analyzer hardware and the signals being probed. It samples the signals and converts them into a digital data stream for the protocol processing engine.

2. **Protocol Packetizer**: Leverages protocol specific data matching algorithms to organize the incoming data stream into protocol-specific packets. It also stores them in the on-board memory.

3. **Hardware trigger and/or filter**: Matches the protocol packets against preset or user-definable patterns and takes the appropriate action.

4. **On board memory:** Some protocol analyzers do not require on-board memory and simply stream the data to the analysis PC. Most high-speed protocol analyzers require large on-board memory to store the processed protocol packets.

5. **Upload interface:** Provides the interface between the protocol analyzer and the analysis PC. It reads the data from the on-board memory and uploads it to the analysis PC for processing and display.

Front-End Implementations in Protocol Analyzers

The primary role of the analyzer's front-end is to serve as the primary interface to the signal being probed, with minimal affect on the signals' electrical or logical characteristics. In addition, it provides a mechanism for signal capture and time synchronization with the protocol packetizer. With the wide adoption of high-speed serial bus technologies such as USB, PCI Express, SAS, and SATA, the front-end implementation has played a pivotal role in protocol analyzers. In these scenarios, the front-end translates the analog signal from the serial domain into the digital data stream to be consumed by the protocol packetizer. The rapid increase

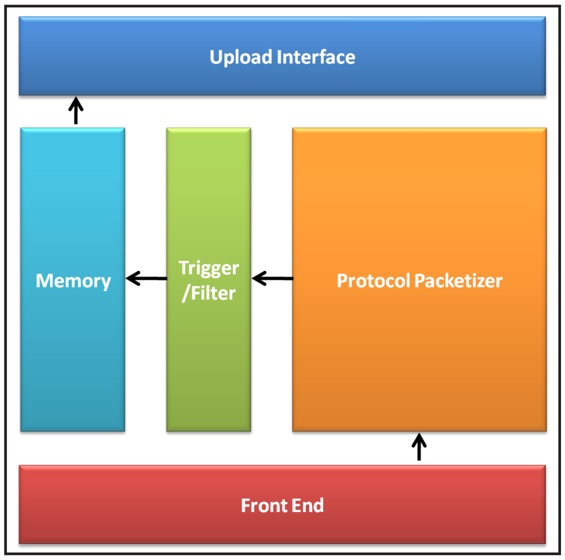


Figure 2: Protocol Analyzer Block Diagram

in bus speeds presents significant challenges in probing and capturing high-speed serial buses.

There are benefits and trade-offs to consider when using different implementation techniques in designing the front-end for a SuperSpeed USB 3.0 protocol analyzer. The most common techniques used for tapping the signal/bus under test include:

- High-impedance, non-intrusive tap
- Active repeater

Designing a non-intrusive tap for high-speed serial buses is becoming more difficult and cost prohibitive. The increase in the SuperSpeed USB signal speeds, reduced bus voltage swing, and noise margin directly contribute to these challenges. Furthermore, as the protocol analyzer sits between the host and the device, the signal integrity can be degraded. Many factors affect signal integrity including the cables, the connectors introduced by the analyzer, and the traces routing the signal from one port to the other on the protocol analyzer itself.

In addition, a high-impedance tap into the analyzer's receiver circuitry can create an impedance mismatch along the signal traces, thereby degrading the signal further. If a 50Ω terminated passive tap is used, the signal can be cut by 50%. Figure 3 illustrates a non-intrusive high-impedance tap implementation.

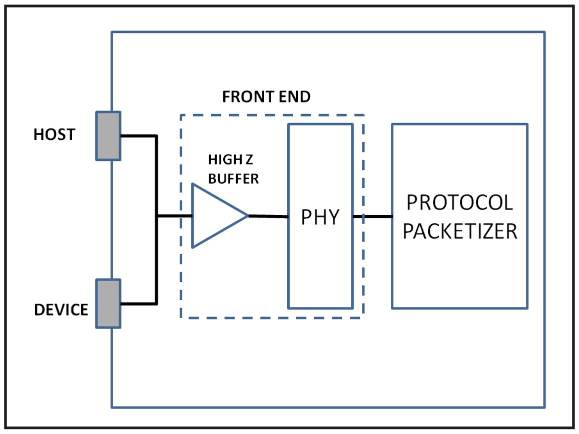


Figure 3: Non-Intrusive High-Impedance Tap

In contrast, active repeater-based implementations do not experience the same signal degradation. Figure 4 shows an example of a repeater-based analyzer front-end.

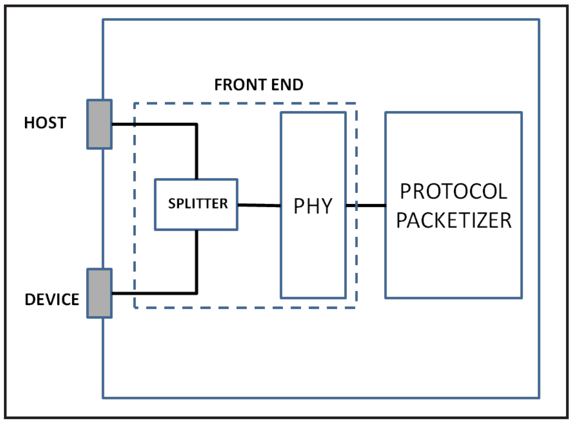


Figure 4: Active Repeater Tap

When designing a repeater based tap one must take caution with certain implementations. Some repeater implementations re-transmit the signal on the bus, and also re-time the signal. Re-timing a signal can adversely affect the spread spectrum characteristics of a signal or potentially interfere with the low-level functionality such as bit locking. In addition, a repeater-based implementation should be designed to minimize any signal latency as it may affect the protocol timing.

Total Phase Beagle™ USB 5000 Protocol Analyzer Active Repeater Implementation

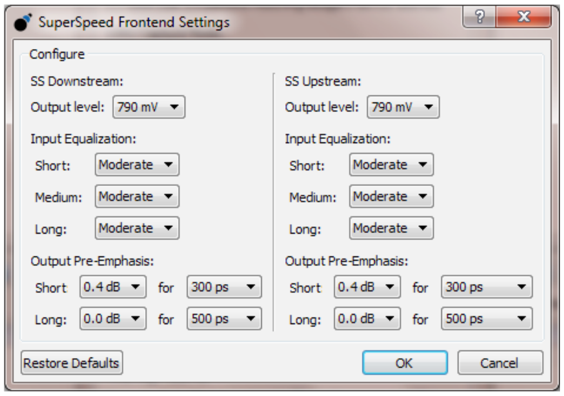
The Total Phase repeater-based implementation in the Beagle™ USB 5000 SuperSpeed Protocol Analyzer employs the best of the implementation techniques discussed. The repeater simply buffers the signal, detects whether a signal is above a certain threshold, and then re-transmits a digital 0 or 1 accordingly. The signal is not re-timed; it is sampled and re-transmitted on the same clock. Finally, the front-end of then Beagle USB 5000 analyzer is designed to minimally affect the signal latency introducing approximately 600ps of latency. As a result, neither the protocol nor its timing requirements are affected.

Since the signal is regenerated, it is possible to modify some aspects of the signal to help developers during the validation and debugging processes. The Beagle USB 5000 analyzer allows users to modify three aspects of the signal properties in either the upstream or downstream direction with the Data Center™ Software (Figure 5).

Output level: Changes the signal levels sent by the transmitter in the Beagle USB 5000 analyzer. By lowering the output signal level, it is possible to test the sensitivity of the USB 3.0 receiver.

Input Equalization: Used to correct for signal degradation due to transmission through a lossy channel. The equalization is broken up into three stages (short, medium, and long), which represents the size of the discontinuity causing the degradation. The equalization settings can correct for minimum, moderate, or maximum amount of degradation or can be turned off.

Output Pre-Emphasis: Intended to address the intersymbol interference (ISI) of high-speed data as it passes through a transmission path. This occurs when the serial stream contains a number of bit times of the same value, then followed by short bit times of the opposite value. The transmission path capacitance is allowed less time to charge



Configure

	SS Downstream:	SS Upstream:
Output level:	790 mV	790 mV
Input Equalization: Short:	Moderate	Moderate
Medium:	Moderate	Moderate
Long:	Moderate	Moderate
Output Pre-Emphasis: Short	0.4 dB for 300 ps	0.4 dB for 300 ps
Long:	0.0 dB for 500 ps	0.0 dB for 500 ps

Figure 5: Total Phase Data Center^{TM} Software SuperSpeed Front-End Settings

due to a shorter bit time resulting in a lower signal amplitude. The output pre-emphasis function of the Beagle USB 5000 boosts the signal sent by the transmitter as needed to compensate for ISI related signal degradation. Pre-emphasis is broken up into two stages (short and long). For each stage, the level (in dB) and the decay (in ps) of boost can be configured. For the most part, the default settings are adequate for most scenarios and do not need to be changed.

Addressing common challenges posed by active repeaters

Active repeater implementation is becoming more acceptable amongst users, but there are common scenarios where the use of active repeater front-end implementation can show erroneous results. Some of these instances, followed by appropriate corrective actions are discussed below:

1. **A device fails to perform when directly connected to the host but appears to work fine when connected to the host via the protocol analyzer.**
   More than likely, this scenario is caused by signal integrity marginalities on either the device or the host. The active repeater is compensating for the signal integrity issues and the device appears to behave normally because the analyzer is connected in-line. It is recommended that the host and the device be evaluated to check for adherence to the physical layer compliance.

2. **Protocol analyzer receives and displays corrupted data.**
   This scenario is potentially caused by sensitivities at the physical interface between the analyzer and the host or the device. Since the active repeater's receiver equalization settings are not dynamically set, it is recommended for users to use shorter cables tor change the repeater settings.

3. **Protocol analyzer sees good data but the host or the device is sending LBAD or LRTY.**
   These errors may be caused by the signal level degradation at the host or device receiver. In this case, using shorter cables and increasing the output levels of the analyzer repeater are recommended.

The rapid increase in bus speeds is presenting significant challenges to developing cost-effective yet high-performance, non-intrusive probes for protocol analysis tools. However; active repeater implementations are becoming more popular as they present the best price/performance alternative. The Beagle USB 5000 SuperSpeed Protocol Analyzer's active repeater implementation provide users with the superior tools necessary to meet the validation and debugging challenges of USB 3.0.