

PGY-SSM SD/ SDIO/eMMC Protocol Analyzer



PGY-SSM SD/SDIO/eMMC Protocol Analyzer is a comprehensive Protocol Analyzer with multiple features to capture and debug communication between host and memory under test. PGY-SSM Protocol Analyzer supports SD, SDIO, and eMMC for data rates up to 200MHz DDR mode. PGY-SSM is the industry's first eMMC protocol analyzer that supports versions 4.41, 4.51, 5.0, and 5.1 specifications. The innovative active probe has minimum electrical loading on the device under test (DUT) and allows protocol data capture without affecting the performance of the DUT. In an industry- The first feature, the PGY-SSM protocol analyzer allows continuous streaming of protocol data from the PGY-SSM Protocol Analyzer to the host system (using USB3.0 or GbE interface) running the UI. Comprehensive decoding of protocol data, command units, and real-time error analysis enables effective verification of communication of SD/SDIO/eMMC host and device.

PGY-SSM Protocol Analyzer enables design and verification engineers to test and debug SD, SDIO, and eMMC by triggering command, response, data, or CRC errors. It also provides instantaneous decoding of Command, Response, CID, CSD, and Ext CSD registers. The analytics feature offers an easy analysis graphical representation of command, response, data, and frequency of operation for the acquired duration.

Key Features

- ❖ Continuous monitoring of protocol data for a long time to capture elusive events (more than 30GB data capture).
- ❖ Analysis of captured data per standards for protocol integrity, count of data bursts, CMD CRC errors, Response CRC errors, Data CRC errors, Timing Values, and Reserved commands.
- ❖ Hardware-based protocol-aware trigger capability in real-time enables capturing specific Events. Triggering facility on patterns, commands, or error events.
- ❖ Users can identify the anomalies by decoding command and response arguments.
- ❖ Analytics feature provides analysis of acquired protocol data by plotting command, response, data, and frequency of operation over acquired time.
- ❖ The analytics feature also provides the decoding of device registers for easy analysis.
- ❖ Filters allow you to view specific packets in decoded protocol packets.
- ❖ Search feature for specific events in protocol activity.

- ✦ Easy-to-use user interfaces save time on the learning curve.
- ✦ Handles long-duration capture and displays the decoded data without demanding extensive resources in the host computer.
- ✦ Inserting markers [using Trigger-In] in protocol activity helps in correlating the input digital signal with Protocol Activity.
- ✦ Trigger-out signal for any specific protocol event allows triggering of other instruments such as an oscilloscope.
- ✦ Interface to host system [running UI] using USB3.0 or Gigabit Ethernet interface.
- ✦ Flexibility to upgrade the hardware firmware using the GbE interface provides easy field up-gradation of the firmware.
- ✦ Export of Decoded data packets to txt file for further analysis.

Specifications

Interfaces Supported	SD3.0 (UHS-I), SDIO4.0, and eMMC 4.41/4.51/5.0/5.1 Specifications
Protocol Decode	Command, Response, CRC, Data, Boot Data, Arguments, Device registers
Data Decode	1 bit, 4 bit, 8 bit SDR, or 4,8 bit DDR
Protocol Test	Protocol Integrity, CRC Errors, Timing values, Data CRC Errors, Reserved commands
Operating Voltage levels	1.8V, 3.3V
Storage Capability	Continuous streaming of protocol activity up to 30GB or 4 to 5-hour capture duration
Capture Mode	Manual Run/Stop, Time-specific
Capture Duration time	1 sec to 5 hours
Trigger on	Command, Response, CRC errors, Sequential trigger
Trigger Actions	Capture data and/or trigger out signal
Signal Input	Digital Signal input to mark the activities in Protocol activity
Protocol Decode	MPHY, UniPro, and UFS layers
Host System Interface	USB3.0 or GbE interface
Host Machine Minimum Requirements	Microsoft Windows® 8, Windows 7, 16GB of RAM. Storage with at least 50 GB HDD space for storing the acquired data. Display with resolution of at least 1024×768

Test Setup



PGY-SSM Protocol Analyzer works on the principle of fat-pipe analysis where the analyzer probes are connected on the interface bus between host and device[memory] of the unit under test. It captures all transactions that are going on between the host/device and does real-time analysis for errors + a detailed analysis of the captured data which is made available through UI running on a host system. Captured data is stored in the hard disk of the system running UI, enabling a long capture [expect to have enough free space in the hard disk].

PGY-SSM Protocol Analyzer interfaces to host using USB3.0 [Super Speed] and GbE. PGY-SSM analyzer & UI software runs in the host machine. PGY-SSM protocol analyzer also has the capability to capture boot data for eMMC.

Probing

PGY-SSM Protocol Analyzer has an active probe, which provides very flexible probing with minimum electrical loading of DUT. This is specifically designed keeping to address challenges in probing eMMC/SD/SDIO signals. The probe supports 200MHz DDR bandwidth so that eMMC/SD/SDIO signals can be captured without any error. Probes have a flying probe lead set with a berg post connector and solder-able probe tips making it very convenient to connect to DUT.

Comprehensive Protocol Analysis

PGY-SSM Software provides the industry's best protocol analysis capabilities. A simple-to-use interface reduces the complexities and time for protocol debugging. Time-stamped view of decode listing provides a complete view of protocol activities between host and device. By clicking on selection prompts, the user can get the decode of arguments, CSD, CID registers, data activities, and more [detailed view]

PGY-SSM SD/SDIO/eMMC PROTOCOL ANALYZER

File About

CONNECT SETUP ANALYZE ANALYTICS REPORTS STOPACQ

SEARCH Type FILTER ADVANCED FILTER

S#	Time	Cmd / RES / DATA / EVEN	Type	Abbreviation	Argument	CRC	EndBit	BusMo	Freque	PWR S	Timing Valu	Errors
1	0s	CMD Line goes low										
2	2.400µs	Boot Mode Active										
3	5.681ms	BOOT_ACK						SDR4				
4	5.971ms	BOOT_DATA[1231 blocks]						SDR4				
5	7.200µs	CMD Line goes high						SDR4				
6	509.507n	CMD0	BC	GO_IDLE_STATE	0x00000000	0x4A	1	SDR4	20MHz			Pass
7	511.407n	CMD8	ADTC	SEND_EXT_CSD	0x000001AA	0x43	1	SDR1	400kHz	Ncc = 759		No response
8	512.207n	CMD55	AC	APP_CMD	0x00000000	0x32	1	SDR1	400kHz	Ncc = 272		No response
9	513.887n	CMD0	BC	GO_IDLE_STATE	0x00000000	0x4A	1	SDR1	400kHz	Ncc = 624		Pass
10	515.787n	CMD1	BCR	SEND_OP_COND	0x00000000	0x7C	1	SDR1	400kHz	Ncc = 712		Pass
11	515.927n	R3 (index = 63)		OCR_REGISTER	0x00FF8080	0x7F	1	SDR1	400kHz	Nid = 8		Pass
12	516.947n	CMD1	BCR	SEND_OP_COND	0x40300000	0x5B	1	SDR1	400kHz	Nrc = 360		Pass
13	517.087n	R3 (index = 63)		OCR_REGISTER	0x00FF8080	0x7F	1	SDR1	400kHz	Nid = 7		Pass
14	518.127n	CMD1	BCR	SEND_OP_COND	0x40300000	0x5B	1	SDR1	400kHz	Nrc = 368		Pass
15	518.247n	R3 (index = 63)		OCR_REGISTER	0x00FF8080	0x7F	1	SDR1	400kHz	Nid = 5		Pass
16	519.287n	CMD1	BCR	SEND_OP_COND	0x40300000	0x5B	1	SDR1	400kHz	Nrc = 368		Pass
17	519.427n	R3 (index = 63)		OCR_REGISTER	0x00FF8080	0x7F	1	SDR1	400kHz	Nid = 7		Pass
18	520.467n	CMD1	BCR	SEND_OP_COND	0x40300000	0x5B	1	SDR1	400kHz	Nrc = 368		Pass
19	520.587n	R3 (index = 63)		OCR_REGISTER	0x00FF8080	0x7F	1	SDR1	400kHz	Nid = 5		Pass
20	521.627n	CMD1	BCR	SEND_OP_COND	0x40300000	0x5B	1	SDR1	400kHz	Nrc = 368		Pass
21	521.767n	R3 (index = 63)		OCR_REGISTER	0x00FF8080	0x7F	1	SDR1	400kHz	Nid = 7		Pass
22	522.807n	CMD1	BCR	SEND_OP_COND	0x40300000	0x5B	1	SDR1	400kHz	Nrc = 368		Pass
23	522.927n	R3 (index = 63)		OCR_REGISTER	0x00FF8080	0x7F	1	SDR1	400kHz	Nid = 5		Pass
24	523.967n	CMD1	BCR	SEND_OP_COND	0x40300000	0x5B	1	SDR1	400kHz	Nrc = 368		Pass

EVENTS USER EVENTS

Time	Event	Duration
0s	CMD Line goes low	
2.400µs	Boot Mode Active	
5.681ms	BOOT_ACK	
7.200µs	CMD Line goes high	
578.689ms	CMD6	
578.829ms	Busy Asserted	
578.869ms	Busy Deasserted	40.000µs
589.909ms	CMD6	
590.029ms	Busy Asserted	
590.049ms	R1b (index = 6)	
590.229ms	Busy Deasserted	199.976µs
591.689ms	CMD6	

Argument Details

[31:0] = 000000000000000000000000100100000000b
 Btl(31) = 0b:OUT_OF_RANGE(no error)
 Btl(30) = 0b:ADDRESS_MISALIGN(no error)
 Btl(29) = 0b:BLOCK_LEN_ERROR(no error)
 Btl(28) = 0b:ERASE_SEQ_ERROR(no error)
 Btl(27) = 0b:ERASE_PARAM(no error)

Statistics

CMD - 10026 Read Cycle - 4618
 RES - 9997 Write Cycle - 145
 CMD CRC - 1 Data Read - 104459kB
 RES CRC - 0 Data Written - 1148kB
 TUN PAT ERR - 0

Offline Mode Live Mode

Protocol Data Capture and Trigger

PGY-SSM Protocol Analyzer has powerful protocol-aware trigger capabilities that allow the capture of protocol events at specific events. PGY-SSM supports simple and advanced trigger capabilities. PGY-SSM can trigger specific command, response, and CRC error conditions. Advanced trigger capabilities allow sequential trigger conditions to capture protocol data after a sequence of events. In Auto mode, data is captured by pressing the RUN button.

Protocol data capture duration is controlled by manual stop or setting the capture duration. Manual stop offers the flexibility of set protocol data capture by visual activities in DUT. In time duration user set data capture in secs to 3 to 4 hours. During the capture mode, protocol data is continuously streamed to the host system hard disk drive for storage.

PGY-SSM SD/SDIO/eMMC PROTOCOL ANALYZER

File About

CONNECT SETUP ANALYZE ANALYTICS REPORTS RUN

Acquisition Setup Custom Display

ACQUIRE

CMD

CMD & Data (D0..D7)

CMD and D0

TRIGGER MODE

Auto

Simple

Advanced

External/Event

CAPTURE DURATION

Manual Stop

Duration

HH : MM : SS

00 : 00 : 35

TRIGGER POSITION

20 %

Advanced Trigger

Seq#	Type	Index	Action	Argument
1	Cmd	23	GOTONEXTSEC	<input type="checkbox"/>
2	Cmd	18	ACQUIRE	<input type="checkbox"/>

Analysis complete. Offline Mode Live Mode

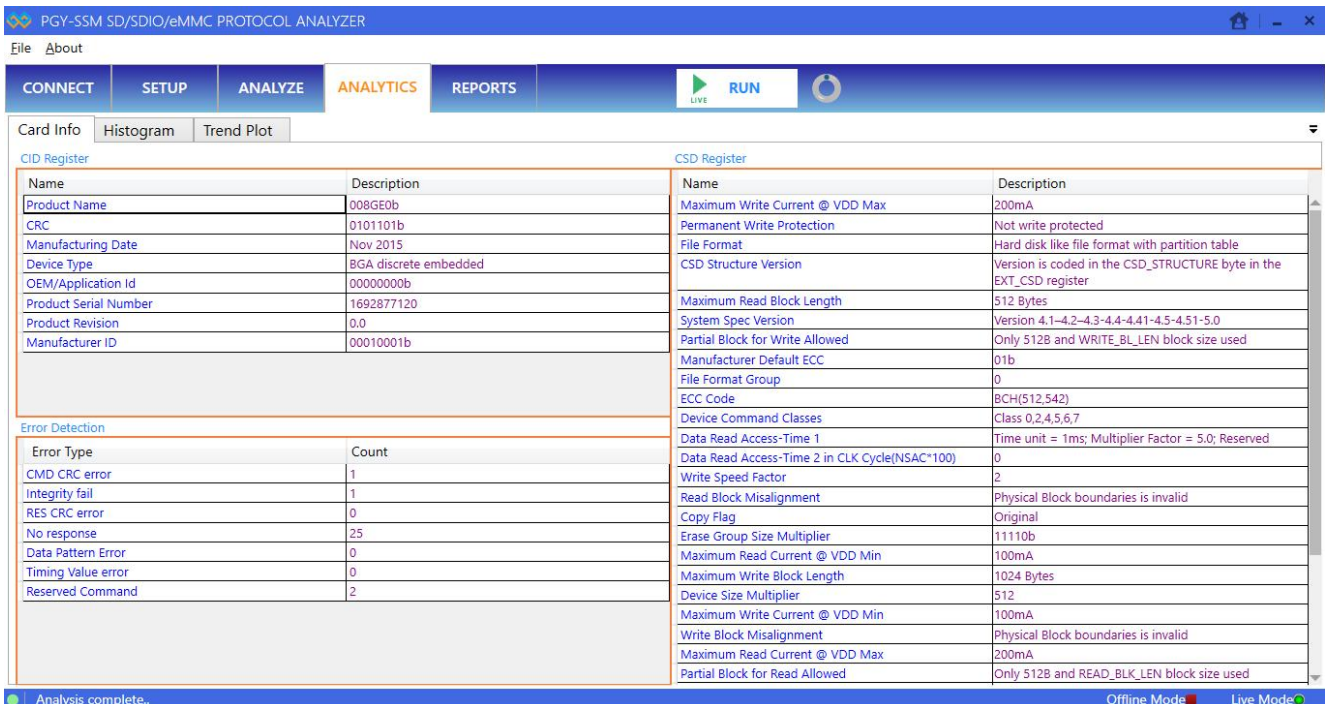
Analytics

A) Analytics features quickly provide insight into protocol activity without going through the complete protocol activity. A sample plot is shown below:



The Analytics view is a bird's eye view of protocol activity for the captured long-duration data. It reduces analysis time by viewing plot command, response, data, and frequency of operation of captured data. The user can search for specific commands or responses in the plot.

B) Card/Device Information provides decoding of register argument of device. Now the user no longer needs to manually decode each register value.



CID Register		CSD Register	
Name	Description	Name	Description
Product Name	008GE0b	Maximum Write Current @ VDD Max	200mA
CRC	0101101b	Permanent Write Protection	Not write protected
Manufacturing Date	Nov 2015	File Format	Hard disk like file format with partition table
Device Type	BGA discrete embedded	CSD Structure Version	Version is coded in the CSD_STRUCTURE byte in the EXT_CSD register
OEM/Application Id	0000000b	Maximum Read Block Length	512 Bytes
Product Serial Number	1692877120	System Spec Version	Version 4.1-4.2-4.3-4.4-4.41-4.5-4.51-5.0
Product Revision	0.0	Partial Block for Write Allowed	Only 512B and WRITE_BLK_LEN block size used
Manufacturer ID	00010001b	Manufacturer Default ECC	01b
Error Detection		File Format Group	0
Error Type	Count	ECC Code	BCH(512,542)
CMD CRC error	1	Device Command Classes	Class 0,2,4,5,6,7
Integrity fail	1	Data Read Access-Time 1	Time unit = 1ms; Multiplier Factor = 5.0; Reserved
RES CRC error	0	Data Read Access-Time 2 in CLK Cycle(NSAC*100)	0
No response	25	Write Speed Factor	2
Data Pattern Error	0	Read Block Misalignment	Physical Block boundaries is invalid
Timing Value error	0	Copy Flag	Original
Reserved Command	2	Erase Group Size Multiplier	11110b
		Maximum Read Current @ VDD Min	100mA
		Maximum Write Block Length	1024 Bytes
		Device Size Multiplier	512
		Maximum Write Current @ VDD Min	100mA
		Write Block Misalignment	Physical Block boundaries is invalid
		Maximum Read Current @ VDD Max	200mA
		Partial Block for Read Allowed	Only 512B and READ_BLK_LEN block size used



Ordering Information

The ordering information is as follows:

PGY-SSM SD, SDIO, and eMMC Protocol Analyzer

(Shipment includes Hardware, software CD, one set probe, USB3.0, an Ethernet Cable, and power adapters)

Options:

PGY-SSM-S/W offline SD, SDIO, eMMC Protocol Analysis Software

(Shipment includes software CD with USB key for license)

Warranty:

Hardware and software carry a warranty of one year.

Probes are covered three-month warranty for any manufacturing defects

Contact Information



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About Prodigy Technovations Pvt Ltd

Prodigy Technovations Pvt Ltd (www.prodigytechno.com) is a leading global technology provider of Protocol Decode, and Physical layer testing solutions on test and measurement equipment. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol decode and physical layer testing solutions that span the serial data, telecommunications, automotive, and defense electronics sectors worldwide.